

## TITLE OF THE INVENTION

## Wireless Boundary Proximity Determining and Animal Containment Apparatus and Method

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part of Application No. 09/499,948, filed February 8, 2000, and claims the benefit of U. S. Provisional Application No. 60/181,098, filed February 8, 2000.

**STATEMENT REGARDING FEDERALLY SPONSORED  
RESEARCH OR DEVELOPMENT**

Not Applicable.

## BACKGROUND OF THE INVENTION

## 1. Field of Invention

16 The invention relates to a method and apparatus for generating and  
17 sensing an electromagnetic field defining a wireless boundary. More specifically,  
18 this invention relates to a method and apparatus for determining the proximity  
19 of a receiver to an electromagnetic field boundary generated by a wireless  
20 transmitter, especially for animal containment.

## 2. Description of the Related Art

23 The present invention relates in general to proximity monitoring systems  
24 for determining when a second device (i.e., receiver module) is proximate to a  
25 first device, (i.e., transmitter), (which is the functional equivalent to determining  
26 when a second device is proximate to a wireless boundary encompassing and  
27 defined relative to the location of the first device) and is particularly directed to a  
28 high sensitivity, low cost proximity detection system which employs a  
29 modulated, quasi-static magnetic field and requires a small, very low cost and  
30 very low power second device as in a wireless pet containment application.

31 Proximity detection devices are used in a variety of applications for  
32 determining the relative nearness of an object, animal or person to a designated

1 area or location or to the location of another object or person. One important  
2 area of application would be to determine if a child strays too far away from a  
3 certain location or from a parent or guardian. Another application would be to  
4 determine if an institutionalized individual or a tagged equipment item has  
5 strayed or been carried away from a designated area. Still another important  
6 area of application would relate to determining when a device is proximate to a  
7 kiosk for the purpose of establishing wireless communications only when the  
8 proximity is a prescribed distance. Still another important application would be  
9 for a pet containment system where a device worn by the pet must self-detect  
10 when it is proximate to a fixed wireless boundary.

11 Prior art methods for these types of proximity detection applications can  
12 generally be classified according to whether an implementation of the proximity  
13 detection method requires the second device (typically the portable, mobile  
14 device) to have both transmit and receive functionality or whether the method  
15 can be implemented with a receive-only second device. Examples in the prior art  
16 of systems requiring both transmit and receive functionality in the second device  
17 include those methods which rely on the transit time or phase shift properties of  
18 an ultrasonic or radio frequency signal. One major disadvantage of all such prior  
19 art methods is the relatively low battery life resulting from the relatively high  
20 power dissipated when the device is transmitting. Other major disadvantages are  
21 the relatively higher cost and larger size required for implementing transmit and  
22 receive functionality as compared to implementing a receive only device.

23 Proximity detection methods which can be implemented with a receive  
24 only second device can generally be sub-classified as systems which determine  
25 proximity by detecting the received signal strength of a propagating radio  
26 frequency signal (typically above a few hundred kHz) or systems which  
27 determine proximity by detecting the received signal strength of quasi-static,  
28 low-frequency (below 500 kHz and more typically below 100 kHz) magnetic field  
29 signal. The accuracy and repeatability of proximity detection based on radio  
30 frequency received signal strength is generally known in the prior art to be  
31 severely affected by multipath reflections from stationary or mobile reflecting  
32 surfaces and by field distortion variations caused by antenna proximity to

1 conductors such as body tissue. Consequently these kinds of methods are not  
2 generally suitable for most proximity detection applications including wireless  
3 pet containment.

4 One prior art proximity monitoring system based on quasi-static magnetic  
5 fields is the wireless pet containment method of Weinberg which employs a  
6 stationary, unmodulated 1-axis magnetic field generator and a pet-worn receiver  
7 that requires a multiplicity of 1-axis sensing antennas and a corresponding  
8 multiplicity of single conversion receivers to form a measure of the incident  
9 magnetic field that is substantially independent of the receiver orientation. Major  
10 disadvantages of this method are the increased receiver circuit complexity, cost,  
11 size and battery current associated with the requirement for a multiplicity of  
12 sensors and receiver channels. Also, this method for detecting the signal  
13 strength of an unmodulated carrier cannot achieve very low noise bandwidths  
14 needed for maximum receiver sensitivity unless tightly matched and expensive  
15 oscillator crystals are used in both the signal generator and receiver. Another  
16 proximity monitoring system based on quasi-static magnetic fields is the child  
17 monitoring method of Belcher which employs a plurality of orthogonal magnetic  
18 fields modulated in a time sequential fashion using on-off amplitude keying at  
19 rates in excess of 1 kHz. This method also requires a multiplicity of receiver  
20 sensor antennas and a corresponding multiplicity of receivers to achieve an  
21 orientation-independent proximity detection performance. It therefore suffers the  
22 same disadvantages of increased complexity, size, battery current and cost. Also  
23 the relatively fast response time required to amplitude demodulate the on-off  
24 keyed carrier is not compatible with achieving the very low noise bandwidths  
25 needed to maximize receiver sensitivity.

26 There remains a need for a proximity monitoring and wireless pet  
27 containment system based on low-frequency magnetic fields and having  
28 minimum receiver size and cost in addition to maximum receiver sensitivity and  
29 battery life.

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## 1                   BRIEF SUMMARY OF THE INVENTION

2                 The above discussed prior art problems and limitations are effectively  
3         remedied in the present invention of an improved system for determining when a  
4         receiver is proximate to a wireless boundary encompassing and defined with  
5         reference to the location of a transmitter. The present invention is based on  
6         near-field signal detection of the total power in a low-frequency (10 kHz to 100  
7         kHz), quasi-static 3-axis magnetic field. Quasi-static magnetic fields are  
8         generally known to be immune to the field-strength variability problems that can  
9         occur in systems based on propagating RF fields because of multipath  
10        reflections and severe field distortion by proximate conducting masses such as  
11        body tissue. Operation in the near-field or quasi-static magnetic field zone is  
12        also generally known to be advantageous for wireless boundary proximity  
13        detection because the sharp inverse 6th power proportionality of the magnetic  
14        field power with distance allows for more accurate range thresholding decisions.  
15        The receiver module used to detect the magnetic field in the present invention is  
16        not required to transmit any signals and therefore can have lower cost and  
17        power, much longer battery life and simpler and more compact construction  
18        compared to prior art methods that require the portable device to transmit either  
19        an RF or ultrasonic signal. The receiver module in the present invention uses a  
20        novel single-output, two axis sensing antenna with orientation-independent  
21        response for detecting the total power in a 3-axis magnetic field signal. This  
22        provides for more accurate wireless boundary proximity detection performance  
23        compared to prior art methods using only a single-axis sensing antenna. The  
24        present invention receiver module achieves accurate, orientation-independent  
25        boundary detection using only one, non-multiplexed signal receiver circuit. This  
26        also allows for lower cost and power, longer battery life and simpler and more  
27        compact construction compared to prior art methods that can only achieve  
28        orientation-independent boundary detection through the use of a multiplicity of  
29        single-axis sensing antennas and a corresponding multiplicity of receiver  
30        circuits.

31                 The present invention uses a composite magnetic field which is  
32         continuously broadcast and detected with no time-sequential multiplexing

1 required for either the magnetic field signal generation, reception or detection.  
2 This allows for use of a magnetic field detection process incorporating coherent  
3 filtering to advantageously reject interference signals associated with the power  
4 line frequency of either 50 or 60 Hz. This allows the present invention to be  
5 much less susceptible to common sources of power line interference compared  
6 to prior art methods not incorporating rejection filtering of the power line  
7 frequency. In fact, coherent rejection filtering at the power line frequency is not  
8 possible for the prior art methods that require receiver antenna sequencing or  
9 multiplexing. The present invention uses continuous, coherent binary phase  
10 shift keying (BPSK) modulation signals to modulate a 3-axis magnetic field  
11 which is detected by a direct quadrature conversion receiver that translates the  
12 received signal directly into continuous, coherent quadrature I and Q baseband  
13 components. This method of carrier modulation and down conversion allows for  
14 a lower effective noise bandwidth in the post conversion filter compared to the  
15 noise bandwidths of several kilohertz exhibited by prior art methods based on  
16 magnetic fields modulated in a time sequential fashion using on-off amplitude  
17 keying or modulated using differential phase shift keying (DPSK) at rates in  
18 excess of 1 kHz. Additionally the use of BPSK modulation is generally known to  
19 have theoretically superior intrinsic signal to noise and bit error rate  
20 performance compared to DPSK. A lower receiver noise bandwidth is  
21 advantageous for achieving better signal-to-noise ratio for the magnetic field  
22 measurement resulting in more accurate and higher resolution boundary  
23 detection. The present invention uses digital signal processing of the sampled  
24 baseband signals to further improve the boundary detection accuracy compared  
25 to prior art methods that do not employ digital signal processing. Because the  
26 sigma delta modulators used for 9-bit (8 bits plus sign bit) signal digitization  
27 employ continuous time integration, the digital correlation filters used to process  
28 the baseband data samples have a theoretical performance equivalent to ideal  
29 matched filters for extracting the signals from random noise and for extracting  
30 the separately identifiable 3-axis magnetic field components from the composite  
31 received signal. Digital post processing is also used to advantage in the present  
32 invention for digitally combining the extracted measures of the 3-axis magnetic

1 field components to form an orientation -independent digital measure of the  
2 total magnetic field power, and for additionally filtering the power measure with  
3 a digital moving average filter to achieve an overall receiver system noise  
4 bandwidth on the order of 2 Hz.

5 Compared to prior art methods, the present invention additionally  
6 provides means to detect when the magnetic field rapidly decreases due to a  
7 transmitter sudden failure or loss-of-power. In the case of a pet containment  
8 application, this prevents the pet from being shocked if the magnetic field  
9 transmitter is accidentally turned off or otherwise loses power. Compared to  
10 prior art methods, the present invention additionally provides means to detect  
11 when the received baseband signals are exceptionally noisy. In the case of a pet  
12 containment application, this feature is useful for preventing a high magnetic  
13 field noise level, such as that encountered near an automobile engine, from  
14 being erroneously interpreted as a valid magnetic field power signal. Without  
15 this feature a pet may run into the street near the front of an automobile and  
16 not receive a correction because the detection device has no facility for  
17 distinguishing between a high level of magnetic field noise and a bona fide  
18 containment zone magnetic field signal. The present invention transmitter  
19 integrates all the signal generation circuitry onto a CMOS integrated circuit chip  
20 and can therefore be lower cost and more compact compared to prior art  
21 methods that do not utilize a single chip for all signal generation circuits.  
22 Similarly, the present invention receiver module integrates the entire signal  
23 receiving circuitry onto a CMOS integrated circuit receiver chip and can  
24 therefore be lower cost and more compact compared to prior art methods that do  
25 not use a single integrated circuit receiver chip. The receiver module also  
26 integrates all the digital signal processing circuitry onto a digital CMOS  
27 integrated circuit chip and therefore typically has lower cost and more compact  
28 compared to prior art methods that do not integrate all digital functions onto a  
29 single chip or that implement the digital processing with a general purpose  
30 microprocessor chip.

31 The present invention generally pertains to a system for determining  
32 when a receiver module becomes proximate to any point on a wireless closed

1 boundary, encompassing the position of the transmitter. The transmitter  
2 includes a magnetic field generator continuously broadcasting a composite,  
3 modulated, time-varying magnetic field signal of a particular carrier frequency  
4 and comprises a low-cost CMOS integrated circuit signal generation chip for  
5 generating optimally chosen carrier and modulation signals. The receiver  
6 module includes a totally passive, electrostatically-shielded, single output, two-  
7 axis magnetic field sensing antenna. The sensing antenna output signal is  
8 amplified and downconverted to baseband using an ultra-compact micropower  
9 direct conversion receiver circuit implemented on a low-cost CMOS integrated  
10 circuit receiver chip. The receiver module additionally includes a low-cost,  
11 micropower, CMOS digital integrated circuit chip for digitally processing the  
12 baseband signals with matched filters to obtain an accurate digital measure of  
13 the total power of the broadcast magnetic field incident on the receiver module.  
14 The CMOS digital chip also includes digital means for reliably determining when  
15 the total magnetic field power measure is above or below a predetermined  
16 threshold level and thereby means for determining when the receiver module  
17 location is proximate to the wireless closed boundary defined by points where  
18 the incident magnetic field power is of a value sufficient to cause the receiver  
19 module magnetic field power measure to be equal to the predetermined  
20 threshold level. The CMOS digital chip also has means for activating signaling  
21 devices as required to signal when the receiver module has crossed the wireless  
22 boundary.

23 The transmitter employs means for continuously broadcasting a 3-axis  
24 composite magnetic field having a single carrier frequency modulated using  
25 coherent binary phase shift keying (BPSK). The CMOS signal generation chip is  
26 provided with a master clock oscillator. Making the carrier frequency an integral  
27 multiple of the line power frequency is advantageous for enabling the signal  
28 detection process to have a high degree of rejection of interference from the  
29 power line frequency or any of its significant harmonics. A system clock  
30 frequency of 32,760 Hz also allows the use of simple integral ratio frequency  
31 division for the generation of modulation waveforms having fundamental  
32 frequencies which are integral sub-harmonics of the power line frequency. The

1    3-axis modulation signals are specifically chosen to facilitate a receiver module  
2    digital signal detection process which has a high degree of rejection of  
3    interference at the power line frequency or any of its significant harmonics and  
4    which allows accurate decomposition of the composite received signal into  
5    separately identifiable components corresponding to the separately identifiable  
6    signals broadcast from each transmitter antenna. To this end, a first  
7    modulation signal is a squarewave of fundamental frequency equal to  $\frac{1}{4}$  the  
8    power line frequency and the second and third modulation signals are  
9    orthogonal squarewaves of fundamental frequency equal to  $\frac{1}{2}$  the power line  
10   frequency. Thus, each modulation signal exhibits zero cross-correlation with the  
11   power line frequency or any of its harmonics when cross-correlated over a full  
12   period of the first modulation signal. This property is advantageous for  
13   implementing device digital correlation filters that are highly effective for  
14   rejecting common sources of electromagnetic power line interference signals.  
15   Also, a correlation waveform having fundamental squarewave frequency of  $\frac{1}{4}$  the  
16   power line frequency (like the transmitter first modulation signal) exhibits zero  
17   cross-correlation with the transmitter second and third modulation signals when  
18   correlated over a full cycle, irrespective of any particular phase relationship  
19   between the correlation waveform and the signals. This property is  
20   advantageous for implementing simple and robust digital means for phase  
21   locking the receiver module data acquisition clock with the transmitter  
22   modulation signals. The magnetic field is broadcast from the transmitter with a  
23   3-axis orthogonal antenna arrangement implemented with a total of four coils,  
24   each of identical construction for cost-efficient manufacture. The coils are  
25   mounted in a 3-dimensional configuration which may be enclosable by the  
26   smallest possible housing in a symmetric arrangement that effectively excludes  
27   any magnetic field cross-coupling between the orthogonal antenna elements.

28         The sensor output signal is amplified and downconverted to baseband by  
29         an ultra-compact, micropower direct conversion receiver wherein the input RF  
30         preamplifier with optional AGC, master clock oscillator, PLL local oscillator  
31         synthesizer, dual I and Q mixers, dual I and Q baseband filters and dual sigma  
32         delta modulators are all integrated on a low-cost CMOS integrated circuit

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1 receiver chip. Most of the receiver circuit gain stages, including the input  
2 preamplifier, use micropower CMOS operational amplifiers having input stages  
3 formed from lateral PNP bipolar transistors which exhibit negligible flicker noise  
4 at frequencies above 1 kHz and lower input-referred input voltage offset relative  
5 to MOS transistors. The preamplifier AGC is useful for minimizing signal  
6 blocking caused by strong interfering signals that result in signal limiting at the  
7 preamplifier output and for minimizing increases in receiver supply current  
8 associated with large RF signals occurring in the receiver. The dual channel  
9 mixer uses a simple architecture involving two active op amps and four CMOS  
10 transmission gate switches achieving high isolation of local oscillator signals  
11 from the RF input. The receiver chip also includes a master clock oscillator  
12 using a 32,760 Hz crystal that needs to match the transmitter crystal to within  
13 about +/- 200 ppm. A conventional PLL synthesizer with integral frequency  
14 division in the PLL loop and half-integer post divider is used to tune the  
15 receiver's local oscillator frequency to nominally the same as the carrier  
16 frequency of the broadcast magnetic field except mismatch between the first and  
17 receiver module 32,760 Hz crystals. This mismatch is accommodated by using  
18 quadrature I and Q downconversion and demodulation in the receiver. The  
19 baseband filter is a continuous time two-pole RC filter using off-chip capacitors  
20 to achieve a 300 Hz cut-off. A first baseband gain stage provides pin-  
21 programmable gains of 20 or 50 and a second gain stage with pin-programmable  
22 gains of 2,4,8, or 16. The baseline at the output of the first gain stage is  
23 restored with a continuous time restorer loop which achieves a 2 Hz low  
24 frequency bandwidth using a 0.47  $\mu$ F off-chip capacitor. The I and Q baseband  
25 signals are integrated and quantized using dual continuous time sigma delta  
26 first order modulators which convert the integrated I and Q signals to density-of-  
27 pulses digital bit streams clocked out at the 32,760 Hz system clock rate and  
28 downsampled by digital up-down counters on the companion CMOS digital chip.  
29 The sigma delta modulators employ current-mode continuous time integrators  
30 such that digital downsampling of the modulator bit streams can result in data  
31 samples that represent the continuous time integration of the I and Q signals.  
32 This allows the use of simple, but highly accurate digital correlation methods in

1 the companion digital chip that very closely emulates ideal continuous time  
2 matched filter correlation. The CMOS receiver chip also incorporates dual  
3 baseline crossing detectors for detecting every instance of baseline crossing of  
4 the I or Q baseband signals. These detectors comprise latchable comparators  
5 with deadtime control to produce countable pulse streams useful for qualifying  
6 the I and/or Q baseband signals as being exceptionally noisy and therefore  
7 representative of invalid data to be ignored by the boundary proximity detection  
8 logic in the companion CMOS digital integrated circuit chip. The micropower  
9 receiver chip operates reliably over a battery voltage range of 4.5 to 6.0 V and  
10 draws a total 5 V supply current of 74 - 91  $\mu$ A for a tuning frequency range of  
11 10-82 kHz.

12 ~~sub~~ B1 > The receiver module is provided with a low-cost digital CMOS integrated  
13 circuit chip for processing the I and Q sigma delta bit streams and baseline  
14 crossing countable pulse streams produced by the CMOS receiver chip. The  
15 digital circuit includes logic, memory, digital filter and digital arithmetic circuits  
16 for downsampling the downsampling the sigma delta I and Q bit streams to  
17 produce signed 8-bit I and Q data sampled at a rate nominally equivalent to 2X  
18 the power line frequency. The sampling rate clock is obtained by integer division  
19 of the 32,760 Hz system clock where the division ratio is "dithered" to establish  
20 and maintain receiver module phase locking with the phase of the transmitter  
21 modulation signals. The digital chip also provides digital correlation of 8  
22 successive I and Q sampled data sets to extract sets of sample measures of the  
23 separately identifiable portions of the I and Q received baseband signals  
24 resulting from the separately identifiable magnetic field intensity components  
25 broadcast by the transmitter first, second and third antennas. The 8-set  
26 correlations are clocked by a measurement rate clock which is the sampling  
27 clock divided by eight and therefore nominally  $\frac{1}{4}$  the power line frequency. The  
28 correlations are done with a simple and compact digital addition or subtracting  
29 means whereby each I or Q data sample needs to be accumulated only once per  
30 measurement cycle. Although the correlations are done with simple digital  
31 means, the results match very closely with ideal continuous time correlation  
32 since the sigma delta modulators employ continuous time integrators and the

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reference waveforms for matched filter correlation are all symmetric, unit amplitude square waves such that correlation by adding or subtracting is exactly equivalent to continuous time correlation. In addition to providing nearly ideal matched filter extraction of the separately identifiable magnetic field component measures, the correlation filters also provide near ideal rejection of power line interference components because the reference correlation waveforms are coherent and integral sub-harmonics of the power line frequency. Additionally, the correlation filtering process provides complete rejection of any dc components in the I and Q signal samples.

The digital chip also provides for post processing of the I and Q correlation results to obtain first, second and third power measures corresponding to those portions of the received signal power arising respectively from the separately identifiable magnetic field power components broadcast by the transmitter first, second and third antennas. These relative values of the computed power measures is dependent on the orientation of the sensing antenna relative to the direction vector of the incident magnetic field. Computing means is also provided for digitally summing the first, second and third power measures to obtain a digital measure of the total incident magnetic field power which is substantially independent of the orientation of the sensing antenna and therefore useful for accurate and robust wireless boundary proximity detection. The digital chip also provides post processing of certain correlation results to compute quadrature pseudo power variables that are measures of only that portion of the received signal power arising from magnetic field power components broadcast by the transmitter first antenna. Because of the cross-correlation properties previously discussed, these quadrature pseudo power measures exhibit very low sensitivity to power line frequency interference and also very low sensitivity to I and Q signal components corresponding the signals broadcast from the transmitter second and third antennas. These pseudo power measures, therefore, provide a very robust data-based means for dithering the sampling rate clock to achieve and maintain a prescribed phase lock between the phase of the digital chip measurement clock and the phasing of the magnetic field modulation signals. Because the correlation phase locking is

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contd

based on the transmitter first modulation signal, it is important that the two-axis sensor antenna be arranged to have some non-zero response to the component of the magnetic field that is broadcast by the transmitter first antenna, at least during those times that the receiver module needs to be accurately monitoring proximity to the wireless boundary. This is arranged in pet containment applications, for example, by orienting the transmitter 3-axis broadcasting antenna such that the principal axis of the transmitter first antenna is in the horizontal plane and by mounting the receiver module sensing antenna on the pet such that its principal sensing plane is nominally horizontal when the pet is in an upright position from which it might walk or run toward the wireless boundary.

The digital chip also includes an 8-tap moving average digital filter for improving the signal to noise ratio associated with the total magnetic field power measure. The power measures are initially computed at a measurement rate of nominally  $\frac{1}{4}$  the power line frequency or 15 samples per second for the case of 60 Hz power. Thus the averaged power measure from the moving average filter is totally refreshed every 0.533 seconds, and the effective noise bandwidth of the averaged data measurement is on the order of only 2 Hz.

The digital chip also includes logic for comparing the computed total power measure with a fixed preselected threshold to determine if the receiver module is proximate to the wireless boundary corresponding to said fixed threshold and whether the receiver module may be approaching the boundary from inside the boundary or from outside the boundary. Logic is also included for activating appropriate signaling device or devices when the receiver module is determined to be proximate to the boundary. In pet containment applications, the signaling devices would possibly include a beeper for emitting an audible warning beep, and means for applying high voltage pulses to electrodes designed to deliver a correction shock suitable for training the pet to avoid the wireless boundary. In applications such as pet containment where the receiver module is normally activated upon approaching the wireless boundary from the inside, a false alarm condition will occur if the magnetic field suddenly disappears due to a transmitter loss-of-power occurrence. This false alarm situation is prevented

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1 in the present invention by including means on the digital chip to detect an  
2 unusually rapid decrease in the value of the magnetic field total power  
3 measures. The digital chip also includes counters for counting the pulses from  
4 the receiver chip corresponding to baseline crossings of the I and Q baseband  
5 signals to determine if the I and Q data is too noisy to result in a valid total  
6 power measurement. Noisy data is flagged as invalid and is not used to drive  
7 the phase locking dithering loop and is not loaded into the total power measure  
8 moving average filter.

9

10 BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

11 The above-mentioned features of the invention will become more clearly  
12 understood from the following detailed description of the invention read together  
13 with the drawings in which:

14 Figure 1 generally illustrates the wireless pet containment system of the  
15 present invention;

16 Figure 2 is a block diagram of one embodiment of the wireless pet  
17 containment system;

18 Figure 3a is a block diagram of one embodiment of the transmitter;

19 Figure 3b is a set of waveforms of selected signals of the transmitter;

20 Figure 4 is a perspective view of one embodiment of the orthogonal  
21 antenna arrangement;

22 Figure 5a is a perspective view of the geometric axes of the sensing  
23 antenna;

24 Figure 5b is a vector diagram of the magnetic field vectors incident on the  
25 sensing antenna;

26 Figure 6 is a schematic diagram of the sensing antenna showing the  
27 orientation of the two sensing elements;

28 Figure 7a is a front elevation view of the sensing element and circuit  
29 board;

30 Figure 7b is a right side view of the sensing element and circuit board;

31 Figure 7c is a bottom plan view of the sensing element and circuit board;

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1       Figure 8a is a top plan view of the sensing element and circuit board  
2 showing one embodiment of electrostatic shielding;

3       Figure 8b is a front elevation view of the sensing element and circuit  
4 board showing one embodiment of electrostatic shielding;

5       Figure 9a is a block diagram of the receiver circuit of the receiver module;

6       Figure 9b is a block diagram of an optional AGC preamplifier circuit for  
7 the receiver module;

8       Figure 9c is a block diagram of a local oscillator synthesis circuit;

9       Figure 9d is a block diagram of a quadrature mixer circuit;

10      Figure 9e is a block diagram of the baseband gain and filtering circuits;

11      Figure 9f is a block diagram of the first order sigma delta modulator  
12 circuits;

13      Figure 10a is a block diagram of a digital data acquisition and processing  
14 circuit;

15      Figure 10b is a timing diagram showing selected correlation sequences for  
16 an embodiment of a digital processing circuit;

17      Figure 10c is a block diagram showing the algorithms for an embodiment  
18 of a digital processing circuit; and

19      Figure 10d is a truth table for valid data and noisy data.

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## 21                   DETAILED DESCRIPTION OF THE INVENTION

22      A wireless pet containment system generating an electromagnetic field  
23 defining a containment boundary for confining a pet wearing a stimulus module  
24 responsive to the electromagnetic field is illustrated generally at **9** in the figures.

25      The wireless pet containment system determines when a second device (i.e., a  
26 receiver) becomes proximate to any point on a wireless closed boundary. The  
27 closed boundary encompasses the position of a first device (i.e., a transmitter).

28      The transmitter includes a magnetic field generator broadcasting a composite,  
29 modulated, time-varying magnetic field signal of a particular carrier frequency.

30      The wireless closed boundary is defined as the locus of all points at or near  
31 ground level on a path surrounding the transmitter for which the intensity of the  
32 magnetic field broadcast by the transmitter is a particular constant. The

1 receiver includes at least one sensing antenna for producing at least one  
2 electrical signal in response to the incident magnetic field. The receiver sensing  
3 antenna output signal is amplified and downconverted to produce at least one or  
4 more baseband signals using at least one direct conversion receiver means. The  
5 receiver processes at least one of the baseband signals produced by the direct  
6 conversion receiver to form a measure of the broadcast magnetic field intensity  
7 incident to the location of the receiver or a measure of the power or energy of  
8 incident field. The receiver also determines when at least one of the measures is  
9 above or below a predetermined threshold level and produces an output signal  
10 when the receiver is respectively and correspondingly inside or outside the  
11 closed, wireless boundary. Increasing or decreasing the intensity of the  
12 composite magnetic field broadcast by the transmitter varies the expanse of the  
13 closed, wireless boundary.

14 Figure 1 generally illustrates the wireless pet containment system **9** of the  
15 present invention. The illustrated embodiment includes a transmitter **10** acting  
16 to broadcast or transmit a composite time-varying magnetic field **12** that is  
17 incident upon a receiver, or stimulus, module **11**, which is typically attached to  
18 an inanimate or animate object, such as a pet dog **39**. The time-varying  
19 magnetic field **12** defines a wireless confinement boundary around the  
20 transmitter **10**. The receiver module **11** receives and processes the incident  
21 magnetic field **12** to form a measure of the magnetic field average intensity or  
22 power. This measure of magnetic field power is used to determine proximity of  
23 the transmitter **10** in relation to the receiver module **11**. When the distance  
24 between the transmitter **10** and the receiver module **11** reaches a predetermined  
25 distance **20**, a response is generated. In the illustrated embodiment, the  
26 response is a deterrent stimulus that is applied to the pet **39**.

27 One embodiment of the wireless pet containment system **9** is illustrated  
28 in Figure 2. The wireless pet containment system **9** includes a transmitter **10**  
29 having an antenna arrangement **13** of one or more antenna coils for  
30 continuously broadcasting a composite time-varying magnetic field **12**  
31 corresponding to at least one signal applied to the antenna arrangement **13** by  
32 the antenna driver circuits **14**. The antenna driver circuits **14** linearly amplify

1 the signal or signals produced by a signal generator **15**. In the illustrated  
2 embodiment, the signal generator **15** is a silicon complementary metal-oxide  
3 semiconductor (CMOS) integrated circuit (IC). The signal generator **15** of the  
4 illustrated embodiment includes all of the functions for generating the signals to  
5 be amplified and broadcast as the composite time varying magnetic field **12**,  
6 including a transmitter clock generator **16**, a carrier frequency synthesizer **17**, a  
7 modulation signal generator **18**, and at least one signal modulator **19**. Those  
8 skilled in the art will recognize that the essential functions can be implemented  
9 in other ways, including, but not limited to, the use of discrete components. The  
10 clock generator **16** produces a master clock signal applied as the input clock to  
11 the carrier frequency synthesizer **17** and to the modulation signal generator **18**.  
12 In the illustrated embodiment, the carrier frequency synthesizer **17** is digitally  
13 programmable to generate a coherent carrier signal,  $f_c$ , at a particular  
14 fundamental frequency suitable for broadcasting the composite magnetic field  
15 **12**. The same carrier frequency is used to excite each transmitter antenna coil.  
16 One acceptable frequency range for the carrier signal is between 10 kHz and 100  
17 kHz. Those skilled in the art will recognize that other frequencies can be used  
18 without departing from the scope and spirit of the present invention. In one  
19 embodiment, the transmitter carrier frequency,  $f_c$ , is selected to be an integral  
20 multiple of the frequency of the local line power, typically either 50 or 60 Hz. By  
21 using a multiple of the power line frequency, a high degree of rejection of  
22 interference from the power line frequency or any of its significant harmonics is  
23 achieved.

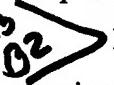
24 The modulation signal generator **18** of the illustrated embodiment  
25 produces a set of one or more separately identifiable waveforms suitable for  
26 modulating the carrier signal through the signal modulator **19** to produce a set  
27 of one or more separately identifiable modulated carrier signals to be amplified  
28 by the antenna drivers **14** and subsequently applied to drive a set of one or more  
29 separately identifiable antenna coils comprising the antenna arrangement **13**.  
30 The set of separately identifiable modulation signals is designed to facilitate  
31 signal processing by the receiver module **11** for accurate and unambiguous  
32 extraction of a set of separately identifiable measures corresponding to the

1 magnetic field components respectively associated with the set of separately  
2 identifiable signals continuously broadcast from the set of separately identifiable  
3 antenna coils.

4 Referring now to the receiver module **11** illustrated in Figure 2, a sensing  
5 antenna arrangement **21** detects the composite time varying magnetic field **12**  
6 broadcast by the transmitter **10** and generates at least one electrical signal that  
7 is received by a receiver circuit **22**. In the illustrated embodiment, the receiver  
8 circuit **22** is a silicon, mixed-signal CMOS integrated circuit. The illustrated  
9 mixed-signal receiver IC **22** includes all of the functions required to receive the  
10 signal from the sensing antenna arrangement **21** and downconvert the signals to  
11 recover the baseband composite modulation components of the received signal.  
12 The illustrated receiver IC **22** includes at least one antenna signal amplifier **23**,  
13 a receiver clock generator **24** for producing suitable local oscillator (LO) signals,  
14 at least one down conversion circuit **25** for recovering the baseband signal from  
15 the amplified antenna signal and filtering and amplifier circuits **38** for  
16 amplification and final filtering of the baseband signal.

17 In the illustrated embodiment, the receiver IC **22** includes at least one  
18 analog-to-digital converter (ADC) **27** to produce digital samples of each of the  
19 baseband signals for subsequent digital signal processing operations. The  
20 illustrated receiver IC **22** includes an optional set of at least one baseline  
21 crossing detector **29** monitoring the set of at least one baseband signal and  
22 producing a single countable pulse for each instance of baseline crossing of the  
23 respective baseband signal. The baseband digital sample data streams **30** and  
24 the baseline crossing countable pulse streams **31** are optionally applied to a  
25 digital signal processor (DSP) **33** acting in concert with a sampling clock  
26 generator **34** to digitally process data streams **30, 31** for the purpose of  
27 extracting and computing an accurate digital measure of the average intensity,  
28 or power, of the incident magnetic field. The input clock signal **28** for the  
29 sampling clock generator is typically supplied from the receiver clock generator  
30 **24**. The magnetic field digital measure produced by the DSP **33** is compared to  
31 a preselected digital threshold value using a proximity detection logic circuit **35**  
32 to determine if the magnetic field sample measure is less than or greater than a

1 preselected threshold value. The threshold comparison results determine  
2 whether the receiver module **11** is located outside or inside a preselected  
3 wireless boundary encompassing the transmitter **10**. A signaling device  
4 activation logic circuit **36** responds to the proximity detection results and  
5 produces signals as required to drive a signaling device **37** that generates a  
6 signal when the receive module **11** moves across the preselected wireless  
7 boundary. In the case of a pet containment application, the signaling device **37**  
8 is typically a stimulus delivery system that produces a deterrent stimulus when  
9 the pet **39** bearing the receiver module **11** crosses from inside to outside the  
10 wireless boundary. In this manner, the wireless pet containment system **9**  
11 trains the pet **39** to remain within the preselected, invisible, wireless boundary.  
12 Those skilled in the art will recognize that the DSP **33**, the sampling clock  
13 generator **34**, the proximity detection logic **35**, and the signaling device  
14 activation logic **36** can be wholly or partially implemented in a number of  
15 different ways without departing from the scope and spirit of the present  
16 invention. For example, they can be wholly or partially implemented on the  
17 mixed-signal CMOS receiver IC **22**, on a separate digital CMOS integrated circuit  
18 chip **32**, or using discrete components.

19  Figure 3a illustrates one embodiment of the transmitter **10** including a  
20 carrier signal generator **15** for the production of three separately identifiable  
21 carrier signals **50**, **51**, and **52**, which are modulated using binary phase-shift  
22 keying (BPSK). Antenna drivers **47**, **48** and **49**, which continuously and  
23 simultaneously excite a 3-axis antenna arrangement **13**, amplify the carrier  
24 signals **50**. The antenna arrangement **13** continuously broadcasts the time  
25 varying, composite magnetic field **12**. The antenna arrangement **13** generally  
26 includes a geometrically orthogonal set of three separate antenna elements  
27 consisting of a first antenna **43** having a principal axis **40** and excited by the  
28 amplified version of a first BPSK modulated carrier signal **50**, a second antenna  
29 **44** having a principal axis **41** and excited by the amplified version of a second  
30 BPSK modulated carrier signal **51** and a third antenna **45** having a principal  
31 axis **42** and excited by the amplified version of a third BPSK modulated carrier  
32 signal **52**. The desired signal voltage amplitudes produced by the antenna

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drivers **47**, **48** and **49** are boosted by exciting the antenna elements **43**, **44** and **45** in a conventional series resonant mode made possible by the use of resonating capacitors **68**, **69** and **70**. The three, separately identifiable BPSK modulated carrier signals **50**, **51** and **52** are generated on the signal generator **15** by the BPSK modulator circuits **53**, **54** and **55**, which modulate a common carrier signal **56** with separately identifiable square wave modulation signals **57**, **58**, and **59**. The modulation signals **57**, **58** and **59** are digitally synthesized from a master clock signal **64** by the respective digital signal generation circuits **60**, **61** and **62**. The frequency synthesis circuit **17** which uses conventional phase locked loop methods for frequency control and includes an analog circuit for making the amplitude of the carrier frequency signal **56** vary in proportion to a reference voltage applied to an amplitude control input **65**, synthesizes the carrier frequency signal **56** from the master clock signal **64**. The carrier frequency **56** produced by the synthesis circuit **17** is tuned to a selected one of numerous possible carrier frequencies using an appropriate *n*-bit digital code applied to the digital frequency control input lines **73**. The *n*-bit digital code controlling the carrier frequency selection is pin-programmed after the signal generator **15** is fabricated. In the illustrated embodiment, the control lines **73** of the signal generator **15** are connected to an off-chip array **71** of *n* connections **72** each of which can be set to a logical "one" or "zero" as desired. Because the carrier signals **50**, **51** and **52** are all produced from the same carrier signal **56**, the magnetic field power components simultaneously broadcast from each of the antenna elements **43**, **44** and **45** are corporately and proportionately increased or decreased by connecting the amplitude control line **65** to an off-chip means for manually adjusting the voltage bias on the amplitude control line **65**. Manual adjustability of the voltage applied to amplitude control input **65** is optionally provided for by connecting the control line **65** to an off-chip voltage divider circuit **66** consisting of a potentiometer connected to the power supply voltage **67** or to some other suitable bias voltage. The expanse **20** of the wireless boundary, defined by the locus of all points on a path surrounding the transmitter **10** for which the total power in the composite magnetic field is a constant, is thus increased by adjusting the voltage divider **66** to effect an

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cont'd

1 increase in the amplitude of the carrier signal **56** and the expanse **20** is similarly  
2 decreased by adjusting the voltage divider **66** to effect a decrease in the  
3 amplitude of the carrier signal **56**.

4       The master clock signal **64** is produced by a suitable clock generator **16**,  
5 such as a CMOS oscillator circuit producing a master clock frequency  
6 corresponding to the mechanical resonant frequency of a common quartz crystal  
7 **63** located off-chip. The resonant frequency of the crystal **63** is chosen to be  
8 nominally 32,760 Hz, which is commonly available from many manufacturers in  
9 small packages at low cost because it can be manufactured as a slightly altered  
10 version of the standard 32,760 Hz "watch" crystal. Further, those skilled in the  
11 art will recognize that numerous possible carrier frequencies in the range of  
12 10 kHz to 100 kHz that are integral multiples of the local line power frequency  
13 (typically either 50 or 60 Hz) are obtainable by applying conventional phase lock  
14 loop synthesis and half-integral-divisor digital frequency divider methods to the  
15 nominal 32,760 Hz master clock signals. By basing the carrier frequencies on  
16 the local power line frequency, the receiver signal processing circuits can reject  
17 extraneous signals generated by the local power lines. Additionally, the use of  
18 the nominal 32,760 Hz master clock frequency allows conventional integral-  
19 divisor digital frequency divider methods to produce fundamental modulator  
20 frequencies that are integral subharmonics of the power line frequency. The  
21 fundamental modular frequencies are useful for the efficient rejection by the  
22 receiver signal processing of any power line interference signals detected by the  
23 receiver sensing antenna **21**. In one embodiment, illustrated in Figure 3b, a first  
24 modulation signal **57** applied to the carrier signal of the transmitter first  
25 antenna **43** is a coherent digital squarewave **57** having a fundamental time  
26 period **74** which is a 4X multiple of the fundamental time period of the power  
27 line frequency such that the fundamental frequency of the first modulation  
28 signal **57** is equivalent to  $\frac{1}{4}$  the fundamental frequency of the power line  
29 frequency. The second BPSK modulation signal **58** applied to the carrier signal  
30 of the transmitter second antenna **44** is in phase alignment with the first  
31 modulation signal **57** and is a coherent digital squarewave **58** having a  
32 fundamental time period **75** which is a 2X multiple of the fundamental time

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1 period of the power line frequency such that the fundamental frequency of the  
2 second modulation signal **58** is equivalent to  $\frac{1}{2}$  the fundamental frequency of  
3 the power line frequency. The third BPSK modulation signal **59** applied the  
4 carrier signal as applied to the transmitter third antenna **45** is also a coherent  
5 digital squarewave **59** which is in phase quadrature with the phase of the  
6 second modulation signal **58** and also has a fundamental time period **76** equal  
7 to the fundamental time period **75** of the second modulations signal **58** such  
8 that both modulation signals **58** and **59** have a fundamental frequency  
9 equivalent to  $\frac{1}{2}$  the fundamental frequency of the power line frequency.

10 With reference now to Figure 4, one embodiment for the physical  
11 configuration of the transmitter 3-axis orthogonal antenna arrangement **12** is  
12 shown. In the illustrated embodiment, a total of four coils **77**, **78**, **82** and **83**,  
13 which are of identical construction for cost-efficient manufacture, are used. The  
14 identical coils are mounted in a 3-dimensional configuration that is enclosed by  
15 the smallest possible housing **80**. The largest inside dimension of the housing  
16 **80** is required to be no larger than the outside diameter of each of the said  
17 identical coils **77**, **78**, **82** and **83**. This configuration is also effective to exclude  
18 any magnetic field cross coupling between the first, second and third antennas  
19 **43**, **44** and **45**. In the illustrated embodiment, the second antenna **44** is split  
20 into two coaxial coils **77** and **78**, and each of the other two antennas **43** and **45**  
21 are implemented using a single coil **82** and **83**, respectively. The coaxial coils  
22 **77** and **78** used for the second antenna **44** define a principal axis **41**. In the  
23 illustrated embodiment the second antenna coils **77** and **78** are sufficiently  
24 spaced to allow the third antenna coil **83** to be fitted between them such that  
25 the third antenna principal axis **42** is aligned orthogonally with and intersecting  
26 with the second antenna principal axis **41**. The arrangement of coils **83**, **77** and  
27 **78** is received within the first antenna coil **82** such that the respective principal  
28 axes **40**, **41** and **42** of the first, second and third antennas **43**, **44** and **45** are all  
29 mutually orthogonal and intersecting. A printed circuit board **79**, which  
30 incorporates the signal generator **15** and the associated components **63**, **66**, **67**  
31 and **71**, the antenna drivers **47**, **48** and **49** and the resonating capacitors **68**,  
32 **69** and **70** is mounted within the antenna arrangement **13**. Because the coaxial

1 coils **77** and **78** are connected in electrical parallel or electrical series to realize  
2 the second antenna **44**, the second antenna **46** will typically have greater or less  
3 circuit inductance than the antennas that use only one coil. Accordingly, the  
4 use of a resonating capacitor **68** having capacitance value respectively smaller or  
5 larger compared to the value of capacitors **69** and **70** is necessary to resonate  
6 the second antenna **44** with the antennas implemented with only a single coil  
7 **82** and **83**.

8 In the illustrated embodiment the operating orientations for the  
9 transmitter antenna arrangement **13** are with the second axis **41** deployed  
10 vertically such that the first antenna **43** which is excited with first modulation  
11 signal **57** is always oriented with corresponding first axis **40** located in a  
12 horizontal plane. Those skilled in the art will recognize that the third axis **42**  
13 can be deployed vertically with a similar effect.

14 With reference to collective Figure 5, the illustrated receiver module **11**  
15 includes a totally passive, two-axis magnetic field sensing antenna **21** producing  
16 a single electrical output signal **100** which is a proportional measure of the  
17 amplitude of  $B_{\text{by}}$ , the projection of the incident magnetic field vector,  $B_r$ , onto the  
18 antenna's sensitive plane defined as the plane which includes the direction  
19 vectors **102**, **104** and **106** and where the output signal **100** is invariant as the  
20 antenna **21** is rotated about its normal axis **102**, said normal axis being  
21 orthogonal to the antenna's sensing plane.

22 Turning now to Figure 6, the two-axis, single output magnetic field  
23 sensing antenna **21** includes two single-axis sensing elements **108a** and **108b**  
24 configured such that (a) the elements **108** have the same sensing axis amplitude  
25 response with said amplitude response being proportional to the projection of  
26 the magnetic field direction vector onto the respective sensing axis **112a** and  
27 **112b** of each element, (b) the transduction responses of the elements **108** to a  
28 magnetic field of carrier frequency,  $f_c$ , have equal scaling factors and a time  
29 domain phase difference of  $90^\circ$ , (c) the elements **108** are mounted such that the  
30 sensing axes **112** are geometrically orthogonal and act to define the antenna's  
31 sensing plane, (d) the elements **108** are mounted such that the element **108a** is  
32 not responsive to the local parasitic magnetic field produced by signal current

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1 flowing in the element **108b** and vice versa, and (e) the single electrical output  
2 signal **100** is produced by the series electrical connection of the output signals  
3 produced individually by the elements **108a** and **108b**. Each element **108** is  
4 made sensitive to the incident time varying magnetic field by the incorporation of  
5 an inductor **110**. The inductors **110** are configured as a series electrical  
6 connection of one or more turns, or loops, with the principal axes of all turns  
7 being co-linear and defining the sensing axes **112**. The coil windings forming  
8 the inductors **110** are directly wound around a bobbin-shaped ferrite magnetic  
9 core material having a small loss tangent at the signal carrier frequency,  $f_c$ .  
10 Those skilled in the art will recognize that the two-axis, single output antenna  
11 **21** can also be realized with other inductor core configurations including a  
12 simple air-core design. As shown in Figure 6, inductors **110a** ( $L_1$ ) and **110b** ( $L_2$ )  
13 are connected in parallel with capacitors  $C_1$  and  $C_2$  respectively forming separate  
14 parallel resonant circuits wherein resistors  $R_{p1}$  and  $R_{p2}$  also respectively  
15 appearing in parallel act to define the electrical response  $Q$ -factors of the parallel  
16 resonant circuits. Inductance values,  $L_1$  and  $L_2$ , and capacitance values,  $C_1$  and  
17  $C_2$  are chosen such that the elements **108a** and **108b** have resonant frequencies  
18 of  $f_{r1}$  and  $f_{r2}$  respectively, such that  $f_{r1} < f_c$  and  $f_{r2} > f_c$ . This produces transduction  
19 responses in the inductors **110a** and **110b** having equal amplitude scaling and  
20  $90^\circ$  time phase difference. In one embodiment, the capacitors are chosen from  
21 capacitors of standard value and the inductors **110a** and **110b** are selected to  
22 have equal inductance values for ( $L = L_1 = L_2$ ), such that capacitors  $C_1$  and  $C_2$   
23 have an average value according to

$$C_{avg} = \frac{1}{(2\pi f)^2(L)} \quad (1)$$

24 and a difference ( $C_1 - C_2$ ) to produce a desired average resonance  $Q$ -factor  
25 defined by the relationship

$$(C_1 - C_2) = \frac{2C_{avg}}{Q_{avg}} \quad (2)$$

1 where  $Q_{avg}$  is the average of the  $Q$ -factors for the elements **108** evaluated at the  
 2 signal carrier frequency,  $f_c$ . The average  $Q$ -factor is also achieved by making the  
 3 total effective parallel resistance  $R_p$  for the elements **108** to have a value of

$$4 \quad R_{p1} = R_{p2} = R_p = \frac{Q_{avg}}{(2\pi f)C_{avg}} \quad (3)$$

5 This total resistance accounts for the total resonant circuit losses, including  
 6 inductor losses, for both winding and core, plus losses in any parallel resistance  
 7 or loading added to control the  $Q$ -factor. Thus, the required  $R_p$  value is actually  
 8 the parallel combination of the parallel-equivalent inductor losses and the  
 9 discrete resistance added as required to realize the required total  $R_p$ .

10 With reference now to collective Figure 7, the one structure for the  
 11 inductors **110** is revealed by the front elevation view of Figure 7a, the right side  
 12 view of Figure 7b and the bottom plan view of Figure 7c. The  $L_1$  sensitive axis  
 13 **112a** is orthogonal to the  $L_2$  sensitive axis **112b**. The inductors **110a** and **110b**  
 14 are aligned so that a line passes through the geometrical and electromagnetic  
 15 center of each inductor **110** to form the antenna's normal axis **102** such that  
 16 the line defining the normal axis **102** is orthogonal to the sensitive axes **112** of  
 17 both inductors **110**. Because of symmetry, the mutual inductance between the  
 18 inductors **110** is eliminated, and any ferrite proximity effect is the same for both  
 19 inductors **110** and is typically on the order of a few percent. The inductors **110**  
 20 and the associated parallel capacitors and resistors are mounted and  
 21 interconnected via a printed circuit board **114**, as illustrated in collective  
 22 Figure 7. The capacitors and resistors are implemented as surface mount  
 23 components for the most compact assembly.

24 With reference now to collective Figure 8, one method of electrostatically  
 25 shielding the antenna **21** is revealed in the top plan view of Figure 8a and the  
 26 front elevation view of Figure 8b. The shield **120** is a partially conductive layer  
 27 completely surrounding the antenna **21**. The sheet resistivity of the partially  
 28 conducting layer **120** is chosen to selectively attenuate the incident electric field  
 29 relative to the incident magnetic field. The sheet resistivity is approximately in  
 30 the range of tens of ohms per square for sensing magnetic field carrier  
 31 frequencies in the commonly used range of 10 kHz to 100 kHz. In the illustrated

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1 embodiment, the shield **120** completely encloses the antenna **21** and is  
2 electrically isolated from all parts of the antenna **21** except for the antenna  
3 output signal conductor, which is considered to be the low-impedance or ground  
4 side connection **122** of the output signal **100**. This is accomplished by  
5 encapsulating the antenna **21** in a non-conductive epoxy and applying an  
6 appropriate coating to the exterior of the epoxy to realize the desired shield **120**.  
7 The high impedance conductor **124** of the output signal **100** is suitably  
8 insulated from the partially conductive coating by a non-conductive sleeve **126**.  
9 The material used to realize the partially conductive selective shield coating is  
10 one of the several graphite-based formulations commercially available as a  
11 quick-drying aerosol for spray application or as a colloidal suspension for  
12 dipping or brush application. Those skilled in the art will recognize that other  
13 coatings may be used for shielding without departing from the spirit and scope  
14 of the present invention.

15 Figure 9 illustrates one embodiment of the receiver module **11**. The  
16 receiver module includes a CMOS direct conversion integrated circuit receiver as  
17 shown in Figure 9a, an optional AGC loop as shown in Figure 9b, a PLL local  
18 oscillator synthesis circuit as shown in Figure 9c, switching mixer circuits for  
19 downconversion as shown in Figure 9d, baseband gain and filtering circuits as  
20 shown in Figure 9e, and first order sigma delta modulator circuits as shown in  
21 Figure 9f. All the essential functions required for implementing a micropower  
22 direct conversion receiver circuit for processing the BPSK modulated RF output  
23 signal **100** produced by a single output, 2-axis magnetic field sensing antenna  
24 **21** are implemented on a silicon, mixed-signal CMOS integrated circuit receiver  
25 chip **22**, in the illustrated embodiment. The receiver chip **22** includes a  
26 micropower preamplifier circuit **23** for receiving the antenna output signal **100**  
27 and providing a voltage gain of typically 100 over a bandwidth of 1.5 kHz to 90  
28 kHz and drawing less than 10  $\mu$ A average continuous current from a battery  
29 power source **204**. The preamplifier circuit **23** is implemented with an all CMOS  
30 transistor design except for the input stage is implemented from the parasitic  
31 lateral PNP bipolar transistors available in any n-well, bulk CMOS integrated  
32 circuit process. The use of lateral PNP bipolar transistors for the preamplifier

1 input stage minimizes signal-to-noise degradation due to flicker noise in the RF  
2 signal frequency region of interest from 10 kHz to 100 kHz. The preamplifier  
3 input bias current is selected to be less than 50 nA in order to minimize the  
4 signal-to-noise degradation due to shot noise associated with the input base  
5 current of the input bipolar transistor. The preamplifier is implemented with  
6 analog CMOS gain circuits using differential circuit means to achieve power  
7 supply rejection as required to avoid gain variations due to normal changes in  
8 the battery power supply voltage over the useful life of the battery **204**.

9 In the illustrated embodiment, the preamplifier **23** includes an AGC loop  
10 **230** as shown in Figure 9b for the purpose of maintaining linear preamplifier  
11 response in the presence of large overload signals. The illustrated AGC loop **230**  
12 includes a full-wave rectifier circuit **220** to rectify the bipolar preamplifier signal  
13 **206** and a differential input operational transconductance amplifier (OTA) **222**  
14 for comparing the output of the full-wave rectifier **220** to a fixed reference  
15 voltage **224** and driving the gate of Negative-Channel Metal Oxide  
16 Semiconductor (NMOS) transistor **226** connected in parallel with the sensing  
17 antenna output signal **100**. In normal low-signal operation, the output of the  
18 full wave rectifier **220** is smaller than the reference voltage **224** causing the OTA  
19 **222** to drive the gate of the NMOS transistor **226** negative such that the NMOS  
20 transistor **226** is in an "off" state and has no effect on the sensing antenna  
21 output **100**. When the preamplifier output signal **206** is increased to a level  
22 where the output of the full-wave rectifier **220** is comparable to the reference  
23 voltage **224**, the OTA output biases the gate of transistor **226** such that the  
24 transistor's channel conducts, thereby shunting enough antenna signal **100**  
25 away from the preamplifier input to dynamically maintain the preamplifier  
26 output signal **206** at a linear region level corresponding to zero error voltage at  
27 the input of the OTA **222**. The AGC loop response is controlled by the off-chip  
28 loop filter capacitor **228**. The AGC loop **230** is disabled by replacing the loop  
29 filter capacitor **228** with a short circuit such that the NMOS transistor **226** is  
30 maintained in a cut-off state at all times. The AGC loop **230** utilizes analog  
31 CMOS micropower circuits requiring a total battery current of only 4  $\mu$ A and  
32 incorporating differential circuit methods to achieve power supply rejection as

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1 required to avoid loop gain variations due to normal changes in the battery  
2 power supply voltage over the useful life of the battery **204**.

3       The master clock signal **28** for the receiver chip **22** is produced by a  
4 suitable CMOS clock oscillator circuit **24** acting to produce a master clock  
5 frequency corresponding to the mechanical resonant frequency of a common  
6 quartz crystal **202** located off-chip. The resonant frequency of the receiver  
7 module crystal **202** is chosen to be nominally 32,760 Hz. In the illustrated  
8 embodiment, the receiver module crystal **202** is of the same type and  
9 manufacture as the transmitter oscillator crystal **63** so that the transmitter and  
10 receiver module master clock frequencies are matched to within +/- 200 ppm.  
11 As with the transmitter **10**, a receiver module master clock frequency of  
12 nominally 32,760 Hz allows conventional phase lock loop synthesis and half-  
13 integral-divisor digital frequency divider methods to produce numerous possible  
14 carrier frequencies in the range of 10 kHz and 100 kHz which are integral  
15 multiples of the local line power frequency. The clock oscillator circuit **24**  
16 utilizes analog CMOS micropower circuits requiring a total battery current of  
17 only 1  $\mu$ A and is designed to provide a clock output signal **28** having a controlled  
18 duty cycle of 50% +/- 2% for accurate control of the conversion gain of the sigma  
19 delta modulators **13**.

20       The master clock frequency **28** of nominally 32,760 Hz is translated to  
21 the local oscillator, LO, frequency required for tuning the direct conversion  
22 receiver to receive the carrier frequency of the composite magnetic field  
23 broadcast by a local oscillator synthesis circuit **26** shown in Figure 9c. A  
24 micropower phase locked loop **240** is used to translate the master clock  
25 frequency,  $f_{CLK}$ , up to a frequency  $f_{PLL} = (f_{CLK}) \bullet (N_{PLL})$ , where  $N_{PLL}$  is the frequency  
26 division divisor of the PLL loop divider. The PLL output frequency is translated  
27 down to the required  $f_{LO}$  frequency by a half-integer post divider and an  
28 additional  $\div 4$  frequency divider incorporated in the quadrature generator circuit  
29 **244**. The resulting  $f_{LO}$  clock frequency is  $f_{LO} = (f_{CLK}) \bullet (N_{PLL}) \div (N_{POST}) \div 4$ , where  $N_{POST}$  is  
30 the post divider frequency divide ratio. In one embodiment,  $N_{POST}$  is a half-  
31 integer. The quadrature generator **244** provides differential  $f_{LO}$  clock lines **208i**  
32 for clocking the I downconverter **25i** and differential  $f_{LO}$  clock lines **208q** for

1 clocking the Q downconverter **25q**. The **208i** LO clocks are generated in  
2 quadrature with the **208q** LO clocks. The PLL loop filter capacitor **246** is  
3 optionally located off-chip. Also, the 5-bit digital code **250** for selecting  $N_{PL}$  and  
4 the 5-bit digital code **252** for selecting  $N_{POST}$  are optionally moved off-chip to allow  
5 the receiver to be digitally tuned by a set of off-chip jumpers or switches **248**  
6 allowing pin programming of the required divider codes. The LO clock generator  
7 **26** utilizes micropower CMOS analog and digital circuits to achieve a battery  
8 current drain of 8 to 23  $\mu$ A for an  $f_{PL}$  frequency range of 100 to 500 kHz.

9 The BPSK modulated RF preamplifier output signal **206** is downconverted  
10 to baseband using a dual-channel CMOS switching mixer **25** as revealed in  
11 Figure 9d. The RF signal **206** is buffered with a 2X voltage gain **260** to produce  
12 a non-inverted RF signal **266** which is also applied to an inverting buffer **262** to  
13 produce an inverted RF signal path **268**. The non-inverted RF signal **266** and  
14 inverted RF signal **268** are alternately commutated by the switches **264i** at the  
15  $f_{LO}$  rate to produce chopped output signal **210i**. The chopped output signal **210i**  
16 thus produced is equivalent to the multiplication of the RF signal by a  
17 squarewave at the LO frequency. The signal multiplication generates the desired  
18 I baseband difference component corresponding to the BPSK modulation  
19 together with the undesired sum frequency component. Similarly, the chopped  
20 output signal **210q** containing the desired Q baseband component  
21 corresponding to the BPSK modulation is produced by commutating the non-  
22 inverted signal **266** and inverted signal **268** by switches **264q** driven with  $f_{LO}$   
23 signals **208q** which are in phase quadrature with  $f_{LO}$  signals **208i**. The  
24 downconversion mixers **25** utilizes analog and digital CMOS micropower circuits  
25 requiring a total battery current of only 5  $\mu$ A and incorporating differential  
26 circuit methods to achieve power supply rejection as required to avoid  
27 conversion gain variations due to normal changes in the battery power supply  
28 voltage over the useful life of the battery **204**. The differential local oscillator  
29 signal lines **208** are routed in metal 2 traces positioned over a metallic ground  
30 plane **261** implemented in metal 1 for the purpose of reducing parasitic coupling  
31 of the LO signals to the preamplifier input via the integrated circuit substrate or  
32 by electromagnetic coupling.

1       The undesired sum signals and other out-of-band signals and noise  
2 components are removed from the chopped mixer output signals **210** by use of a  
3 dual-channel baseband filtering and amplifier circuits **38**, as illustrated in  
4 Figure 9e. The baseband filter and amplifier circuits **38** are comprised of a  
5 second order low-pass filter **270** containing two passive RC networks, each with  
6 a series 160 k $\Omega$  n-well resistor connected to 3300 pF off-chip capacitors **280** to  
7 produce a 300 Hz low-pass cutoff frequency. A unity gain CMOS operational  
8 amp circuit buffers the output of the first filter from the second filter. The low-  
9 pass filter **270** is followed by a first gain stage **272** and then a second gain stage  
10 **274**. In one embodiment, the voltage gain of the first gain stage **272** is pin-  
11 programmable for gains of 20 or 50 and the voltage gain of the second gain stage  
12 **274** is pin-programmable for gains of 2, 4, 8, or 16 using pin-programming  
13 means similar to the switches **248** in Figure 9c. The output of the first gain  
14 stage **272** connects to a continuous-time baseline restorer circuit **276**, which  
15 holds the dc level of the first gain state output to within a few millivolts of the  
16 desired output dc level, approximately  $\frac{1}{2}$  of the available battery voltage. This dc  
17 feedback circuit **276** acts as a high-pass filter with a -3 dB cutoff frequency of 2  
18 Hz for an off-chip compensation capacitor **278** of 0.47  $\mu$ F. The reduced dc offset  
19 achieved by using lateral PNP bipolar transistors for the input stage of the  
20 second gain stage **274** eliminates the need for a second dc restoration loop to  
21 correct the second gain stage **274**. The dual baseband filtering and amplifier  
22 circuits **38** utilize analog and digital CMOS micropower circuits requiring a total  
23 battery current of 19  $\mu$ A and incorporating differential circuit methods to  
24 achieve power supply rejection as required to avoid baseband gain variations  
25 due to normal changes in the battery power supply voltage over the useful life of  
26 the battery **204**.

27       The filtered I and Q baseband signals **212** are integrated in continuous  
28 time fashion and quantized into density-of-pulses (DOP) bit streams **30** using a  
29 dual-channel sigma delta first order modulator **13** as shown in Figure 9f. A  
30 linear CMOS signal path transconductor **284** converts the baseband signals **212**  
31 to differential current signals **281** that are combined with a switched differential  
32 feedback current signal **283** supplied by the reversible positive-channel metal

1 oxide semiconductor (PMOS) current mirror **286**. The combined differential  
2 current signals **281** and **283** are then converted to a composite single-ended  
3 current signal **285**, which is continuously integrated by an integrator **290**. The  
4 integrator output is monitored by a CMOS comparator **292** which acts in  
5 combination with an up/down control logic **296** to provide proper feedback  
6 control **298** to the reversible current mirror **286**. The feedback control lines **298**  
7 clock the reversible current mirror **286** at the master clock rate **28** such that the  
8 differential feedback current **283** is also clocked at the master clock rate **28** and  
9 has a 1:1 “on” to “off” ratio or a duty cycle of 50%. The polarity of the clocked  
10 feedback current **283** produced by the reversible current mirror **286** is  
11 determined by whether control line **298a** or **298b** is active, the selection of  
12 which depends on whether the integrator output is above or below the input-  
13 referred comparator threshold level **299**. The feedback control is arranged such  
14 that the clocked feedback current results in a negative-going integrator output  
15 for any clock cycle starting when the integrator output is above the reference  
16 threshold level **299** or a positive-going output for any clock cycle starting when  
17 the integrator output is below the reference threshold level **299**. This keeps the  
18 integrator output level within a certain error band of the reference threshold  
19 level **299** and, therefore, results in zero net integrator input current **285** on  
20 average. This implies zero average net charge transfer to the integrator **290** on  
21 average, which implies that the time integral of the feedback current **283** is in  
22 balance with the time integral of the signal current **281** on average. The  
23 feedback current **283** is a 4X multiple of the differential reference current signal  
24 **287** produced by reference transconductor **282**. The reference input voltage for  
25 the reference transconductor **282** is set by an off-chip resistor to allow external  
26 adjustment of the conversion gain of the sigma delta modulator **13**. The  
27 reference transconductor **282** is a replicated copy of the signal transconductor  
28 **284** to render the overall modulator conversion gain of the sigma delta  
29 modulator **13** insensitive to transconductance variations caused by integrated  
30 circuit processing variations or variations in operating temperature. Because a  
31 fixed feedback charge is either removed or added to the integrator for each clock  
32 cycle, the time integral of the feedback current **283** and, therefore, the time

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1 integral of the signal current **281** is measured digitally by appropriately  
2 counting the bit streams **30**. The up/down logic **296** configures the output bit  
3 streams **30** to contain a logic zero for each clock cycle corresponding to a  
4 positive value of the feedback current **283** and a logic one for each clock cycle  
5 corresponding to a negative value of the feedback current **283**. The dual-  
6 channel sigma delta first order modulator **200** utilizes micropower analog and  
7 digital CMOS circuits requiring a total battery current of 19  $\mu$ A and  
8 incorporating differential circuit methods to achieve power supply rejection as  
9 required to avoid modulator conversion variations due to normal changes in the  
10 battery power supply voltage over the useful life of the battery **204**.

11 The receiver IC **22** optionally includes dual baseline crossing detectors **29**  
12 for detecting every instance of baseline crossing of the I and Q baseband signals  
13 **212**. The baseline crossing detector **29i** produces at its output **31i**, a countable  
14 logic pulse for each instance of baseline crossing of the I baseband signal **212i**.  
15 Similarly, the baseline crossing detector **29q** produces at its output **31q**, a  
16 countable logic pulse for each instance of baseline crossing of the Q baseband  
17 signal **212q**. The baseline crossing detectors **29** are implemented using voltage  
18 comparator circuits with latchable outputs such that the comparator outputs  
19 **31** can be clamped high for a fixed deadtime of nominally 1 millisecond  
20 immediately following a detected baseline crossing. The fixed deadtime acts to  
21 limit the maximum output pulse count rate and prevent a high power  
22 consumption that might otherwise occur when detecting very noisy signals  
23 having many baseline crossings. The fixed deadtime also prevents multiple  
24 pulsing at the outputs **31** that may otherwise occur when using low-hysteresis  
25 comparators to detect relatively slow threshold crossings of a noisy signal. In  
26 one embodiment, the nominal 1 millisecond deadtime is generated using a  
27 presetable digital counter to count the master clock **28** for 32 clock cycles. The  
28 dual baseline crossing detectors **29** utilizes micropower analog and digital CMOS  
29 circuits requiring a total battery current of 5  $\mu$ A and incorporates differential  
30 circuit methods to achieve power supply rejection as required to avoid  
31 performance degradation due to normal changes in the battery power supply  
32 voltage over the useful life of the battery **204**.

With reference to collective Figure 10, one embodiment for the receiver module **11** uses a digital CMOS integrated circuit **32** for digital data acquisition and processing as illustrated in Figure 10a, a correlation means for extracting magnetic field component measures from the I and Q data samples using the correlation sequences described in Figure 10b, an arithmetic logic unit (ALU) to digitally compute magnetic field component power and total power measures according to the method revealed in Figure 10c, and a means for data-based correlator phase locking using the logic summarized in the truth table of Figure 10d. Signed 8-bit data **318** representative of the time integration of the filtered I and Q baseband signals **212** is produced by dual sigma delta sampling filters **300** which count the sigma delta bit streams **30** under control of the master system clock,  $f_{CLK}$ , **28** (nominally 32,760 Hz) and the sampling clock,  $f_s$ , **314** generated by the I/Q sample rate generator **34**. The sigma delta sampling filters **300** incorporate digital up-down counters which count up on  $f_{CLK}$  clock **28** if the bit stream **30** is a logic “one” and count down on  $f_{CLK}$  clock **28** if the bit stream is a logic “zero”. Signed 8-bit values in the up-down counters are then read out as digital samples **318** representative of the I and Q baseband signals continuously integrated by the sigma delta modulators **200** over a time equivalent to one period of the  $f_s$  clock **314**. Thus, the up-down counters forming the sigma delta sampling filters **300** are repetitively read out and reset at the  $f_s$  clock rate. The  $f_s$  sampling clock **314** is produced by an I/Q sample rate generator **34** incorporating a frequency divider which divides the system clock **28** by integer divisor  $N_{DIV}$ . The average value of  $N_{DIV}$  is selected to provide an average  $f_s$  clock frequency **314** equal to 2X the local power line frequency. Also, the value of  $N_{DIV}$  (and indirectly the value of  $f_s$ ) are “dithered” under control of data phase locking logic **306**. The  $f_s$  sampling clock **314** is further divided by a conventional divide by 8 binary counter **312** to produce the measurement rate clock,  $f_M$ , **316**. The average  $f_M$  clock **316** frequency is thus regulated to be  $\frac{1}{4}$  the power line frequency or the average period of the  $f_M$  clock **316** is regulated to be nominally the same as the period **74** of the transmitter first modulation signal **57**.

The receiver module digital IC **32** includes noisy data detection logic **310** for determining if the data acquired over an  $f_M$  clock cycle should be flagged as

1 valid data or invalid, noisy data based on the number of I or Q baseline  
2 crossings as detected by the baseline crossing detectors **29**. The noisy data  
3 detection logic **310** includes dual digital counters configured to count the I and  
4 Q cross count bit streams **31** for one period of the  $f_M$  clock and digital logic to  
5 compare each count to an internally stored fixed digital parameter, GOODTHLD.  
6 The comparison logic is configured to produce a true good data 1-bit status flag  
7 **328** if either the I or Q baseline counts over one  $f_M$  period does not exceed  
8 GOODTHLD. A typical value of 10 is used for the GOODTHLD parameter, in one  
9 embodiment.

10 The receiver module digital IC **32** includes digital correlation filters **302**  
11 for correlating the I and Q sampled data **318** to extract sets of sample measures  
12 **320** of the portions of the I and Q received signals resulting from the magnetic  
13 field intensity components broadcast by the transmitter first, second and third  
14 antennas **43**, **44** and **45**. A set of first measures, Y1i and Y1q corresponding to  
15 the content of the I and Q samples **318** associated with the magnetic field  
16 intensity component broadcast by the transmitter first antenna **43** are obtained  
17 by cross-correlating the I and Q samples **318** with the Y1code correlation  
18 waveform **340** of Figure 10b. This is implemented in the digital correlation  
19 filters **302** by digitally cross-correlating of 8 successive sets of the I and Q digital  
20 sample representations **318** with the sequence {+1, +1, +1, +1, -1, -1, -1, -1}.  
21 Similarly, a set of second measures, Y2i and Y2q, which are associated with the  
22 magnetic field intensity component broadcast by the transmitter first antenna  
23 **43** are obtained by cross-correlating the I and Q samples **318** with the Y2code  
24 correlation waveform **342** in Figure 10b. This is implemented in the digital  
25 correlation filters **302** by digitally cross-correlating 8 successive sets of the I and  
26 Q digital sample representations **318** with the sequence {-1, -1, +1, +1, +1, +1, -  
27 1, -1}. Similarly, a set of measures Zi and Zq, which correspond to the content  
28 of the I and Q samples **318** associated with the magnetic field intensity  
29 component broadcast by the transmitter second antenna **44** are obtained by  
30 cross-correlating the I and Q samples with the Zcode correlation waveform **344**  
31 of Figure 10b. This is implemented in the digital correlation filters **302** by  
32 digitally cross-correlating 8 successive sets of the I and Q digital sample

1 representations **318** with the sequence {-1, -1, +1, +1, +1, +1, -1, -1}. Similarly,  
2 a set of measures  $X_I$  and  $X_Q$  corresponding to the content of the  $I$  and  $Q$  samples  
3 **318** associated with the magnetic field intensity component broadcast by the  
4 transmitter third antenna **45** are obtained by cross-correlating the  $I$  and  $Q$   
5 samples with the Xcode correlation waveform **346** of Figure 10b. This is  
6 implemented in the digital correlation filters **302** by digitally cross-correlating 8  
7 successive sets of the  $I$  and  $Q$  digital sample representations **318** with the  
8 sequence {+1, +1, -1, -1, +1, +1, -1, -1}. The 8 successive sets of the  $I$  and  $Q$   
9 digital samples **318** used for all the indicated digital correlation operations  
10 represent the  $I$  and  $Q$  samples acquired over one period,  $T_M$ , of the  $f_M$   
11 measurement rate clock **316** as indicated by Figure 10b. Therefore, on average  
12 the correlations are also performed over nominally one complete cycle **74** of the  
13 transmitter first modulation signal **57**, and over two complete cycles of the  
14 transmitter second and third modulation signals **58** and **59**. In one  
15 embodiment, the digital correlation filters **302** implement the indicated  
16 correlations by digital processing means wherein each of the 8 successive  $I$  and  
17  $Q$  samples is either added or subtracted from a digital accumulator in  
18 accordance with the indicated correlation sequences. This method requires that  
19 each  $I$  or  $Q$  data sample be accumulated only once per measurement cycle,  
20 being therefore implementable with simpler and more compact digital processing  
21 logic compared to prior art correlator methods based on multi-tap digital  
22 transversal filters involving a multiplicity of accumulation operations for each  
23 data sample corresponding to the multiplicity of transversal filter taps. Because  
24 the successive samples are accumulated at the  $f_s$  clock **314** rate, the correlation  
25 results for any particular  $f_M$  clock period, shown as  $I_{10}/Q_0 - I_7/Q_7$  in the data  
26 acquisition pipeline **348** of Figure 10b, are complete at the end of the  $f_M$  period  
27 after the  $I_7/Q_7$  sample set **358** is correlated. The correlation results are then  
28 passed to the ALU **304** for additional processing at the  $f_M$  rate **316** beginning  
29 during the first  $f_s$  clock cycle of the next  $f_M$  clock data correlation period. In one  
30 embodiment, the correlation results **320** are unsigned 8-bit binary values. No  
31 sign bit is necessary because all subsequent processing of the correlation results  
32 **320** involve only squaring operations or addition of absolute values.

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1       The receiver module digital IC **32** includes a digital arithmetic logic unit  
2       **304** for digital arithmetic computations on the I and Q correlation results to  
3       obtain first, second and third power measures corresponding to those portions  
4       of the received signal power arising respectively from magnetic field power  
5       components broadcast by the transmitter first, second and third antennas **43**,  
6       **44** and **45**, the relative magnitudes of said power measures being dependent on  
7       the orientation of the receiver module sensing antenna **21** relative to the  
8       direction vector of the incident field. The digital arithmetic logic unit **304**  
9       provides for digitally summing the first, second and third power measures to  
10      obtain a digital measure, R or  $R_{AVG}$ , of the total magnetic field power incident on  
11      the receiver module **11**, said total power measure being independent of the  
12      orientation of the receiver module sensing antenna **21** and therefore useful for  
13      accurate and robust wireless boundary proximity detection. The arithmetic logic  
14      unit **304** processes the indicated correlation results **320** according to the  
15      arithmetic formula **370** of Figure 10c to produce an accurate first measure, YS,  
16      **382** of that portion of the received signal power arising from the magnetic field  
17      power broadcast by the transmitter first antenna **43**. The arithmetic logic unit  
18      **304** also processes the indicated correlation results **320** according to the  
19      arithmetic formula **374** of Figure 10c to produce an accurate second measure,  
20      ZS, **386** of that portion of the received signal power arising from the magnetic  
21      field power broadcast by the transmitter second antenna **44**. The arithmetic  
22      logic unit **304** also processes the indicated correlation results **320** according to  
23      the arithmetic formula **372** of Figure 10c to produce an accurate third measure,  
24      XS, **384** of that portion of the received signal power arising from the magnetic  
25      field power broadcast by the transmitter third antenna **45**. The digital  
26      arithmetic logic unit **304** is implemented with a 12-bit architecture and include  
27      logic for binary number addition, rotation and truncation. The squaring  
28      operations indicated in Figure 10c are implemented with the Booth procedure  
29      for binary number multiplication. The 16-bit multiplication results are  
30      truncated back to 8-bits for further processing operations.

31 <sup>sub</sup> b3 > The measures XS **384** and ZS **386** represent accurate power measures  
32      only if the receiver module  $f_m$  measurement clock **316** is locked in close phase

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*cont'd*

alignment with the transmitter third modulation signal **59**. However, the power measure YS **382** is accurate irrespective of the phase relationship between the receiver module acquisition and measurement clock,  $f_m$  **316** and transmitter modulation signals. The digital arithmetic logic unit **304** also processes the indicated correlation results **320** according to the arithmetic formula **376** of Figure 10c to produce a first pseudo power measure, Y1S **324a** and for processing the indicated correlation results **320** according to the arithmetic formula **378** of Figure 10c to produce a second pseudo power measure, Y2S **324b**. The pseudo power measures **324a** and **324b** have variable magnitude as a function of the phase of the receiver module  $f_m$  clock relative to the phase of the transmitter first modulation signal **57**, however the variation of measure **324a** is in quadrature relationship with the variation of measure **324b**. Moreover, the magnitudes are equal when the phase of the  $f_m$  clock **316** is aligned with the phase of the transmitter third modulation signal **59** as desired to guarantee the accuracy of power measures **384** and **386** as previously described. Moreover any shift away from this desired phase lock relationship produces an increase in the magnitude of the **324a** pseudo power measure and a decrease in the magnitude of the **324b** pseudo power measure or vice versa. The magnitude difference between the pseudo power measures **324a** and **324b** is therefore useful for application as an error signal in a dithering feedback means of maintaining the desired phase lock between receiver module  $f_m$  clock **316** and transmitter third modulation signal **59**. The frequency of the  $f_s$  sampling clock **314** is dithered by dithering the  $N_{DIV}$  ratio used by the I/Q sample rate generator **34** to produce the  $f_s$  clock. As previously discussed, the  $f_s$  clock is desired to be nominally 2X the power line frequency so that the  $f_m$  clock is  $\frac{1}{4}$  the power line frequency to be in agreement with the frequency of the transmitter first modulation signal **57**. If  $Y2S < Y1S$  as detected by the data phase locking logic **306**, then  $N_{DIV}$  is set to provide an  $f_s$  slightly less than the power line frequency. If the data phase locking logic **306** determines that  $Y2S >$  or  $= Y1S$ , then  $N_{DIV}$  is set to provide an  $f_s$  slightly greater than the power line frequency. If the noisy data detection logic **310** determines that the Y1S and Y2S measures **324** are based on noisy and potentially invalid data, then  $N_{DIV}$  is not dithered, but is held

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at the nominal settings. The dithering data phase lock process uses the  $N_{Dv}$  values as revealed in the truth table 400 of Figure 10d and is effective to acquire the desired data phase locking in about 1 second and to maintain robust locking properties under poor signal-to-noise ratio conditions. To ensure that all 8 sets of I/Q data samples 355 used in a given correlation operation are acquired with the same sampling time 315, the value of  $N_{Dv}$  must be dithered sometime 354 or 362 before the completion of the sample period corresponding to the acquisition of the first data set I0/Q0 352 or 358. This means that the arithmetic logic unit 304 must complete the calculation of the pseudo power measures 324 in less than 8.33 milliseconds (for the case of 60 Hz line power frequency) which corresponds to about 273 cycles of the 32,760 Hz system clock 28. This is achieved using a Booth multiplication procedure that requires only 10 clock cycles for multiplication of 8-bit numbers. Those skilled in the art will recognize other multiplication methods which can be used.

The digital arithmetic logic unit 304 provides digital means 380 for summing the first, second and third power measures 382, 384 and 386 to obtain a digital measure, R, 381 representative of the total magnetic field signal power incident on the receiver module 11. The total power measure 381 is substantially independent of the orientation of the receiver module sensing antenna 21 and therefore useful for accurate and robust wireless boundary proximity detection. The noise-related uncertainty in the total power measure sample values 381 is optionally reduced by additional digital filtering to obtain a more accurate measure of the total magnetic field signal power. This additional digital filter is implemented in the form of a uniformly weighted, 8-tap moving average filter wherein 8 successive R values are stored in data pipeline 388 and all 8 values are summed in an accumulator 390 to provide the more accurate sample measure,  $R_{AVG}$  322. The arithmetic logic unit 304 is configured to monitor the noisy data status flag 328 and load new R values 381 into the digital filter pipeline 388 only if the flag 328 is set to indicate valid data.

The receiver module digital IC 32 includes boundary proximity detection logic 35 which compares the value of the orientation-independent total power measure,  $R_{AVG}$ , 322 to the value of an internally stored, preselected fixed digital

1 parameter, RTHLD. A wireless boundary encompassing and referenced to the  
2 position of the transmitter **10** is defined to be the locus of all points on a path  
3 surrounding the transmitter for which the receiver module computed total power  
4 measure **322** is equal to the fixed RTHLD reference value. The value used for  
5 the fixed parameter RTHLD should be far enough above the noise floor of the  
6  $R_{AVG}$  data **322** to provide for an acceptable signal-to-noise ratio and boundary  
7 proximity detection repeatability when the value of  $R_{AVG}$  approaches the value of  
8 RTHLD. For pet containment applications, RTHLD should be at least four times  
9 greater than the noise floor of the  $R_{AVG}$  signal. By comparing the computed  
10 power measure sample values **322** to RTHLD, the boundary proximity detection  
11 logic **35** unambiguously detects when the receiver module **11** becomes  
12 proximate to the wireless boundary and whether the boundary is approached  
13 from the inside or from the outside. The boundary detection logic **35** provides at  
14 least one logic control signal **330** to the device activation logic **32** as required to  
15 activate a signaling device or devices **37** when, as in a pet containment  
16 application, the receiver module **11** approaches the wireless boundary from the  
17 inside as indicated by the detection of  $R_{AVG} < RTHLD$  for one or more consecutive  
18 measurement cycles. Alternately, the boundary detection logic **35** may act to  
19 provide logic control signal or signals **330** to the signaling device activation logic  
20 **36** as required to activate a signaling device or devices **37** when, as in a kiosk or  
21 collision avoidance application, the receiver module **11** approaches the wireless  
22 boundary from the outside as indicated by the detection of  $R_{AVG} > RTHLD$  for one  
23 or more consecutive measurement cycles. For pet containment applications, the  
24 boundary control logic **35** compares the total power measure **322** to two  
25 different fixed threshold levels for the purpose of defining a wireless warning  
26 boundary for warning the pet **39** before it reaches the primary containment  
27 boundary which the pet **39** has been trained to associate with negative  
28 correction stimulus such as a mild shock. Depending on the application, the  
29 signaling device activation logic **36** activates the signaling device or devices **37**  
30 including one or more of a sonic (audible by humans and pets) sound emitter,  
31 an ultrasonic sound emitter, a visible light emitter, high voltage pulses via  
32 exposed electrodes, emitter of chemical vapor, aerosol or spray, RF signal

1 transmitter, or mechanical vibration emitter.

2 In those applications, such as pet containment, where the boundary

3 detection logic **35** and device activation logic **330** are configured to activate a

4 signaling device or devices **37** when the receiver module **11** and pet **39** approach

5 the wireless boundary from the inside, a false alarm condition can occur when

6 the  $R_{AVG}$  data measure suddenly drops below RTHLD due to a sudden loss-of-

7 power to the transmitter **10**. For these applications, the receiver module digital

8 IC **32** includes a loss-of-power detection logic circuit **308**, which compares the

9 current total power measure,  $R$ , **381** with one of the earlier  $R$  values as stored in

10 the R0-R7 data pipeline **388**, and sets a 1-bit loss-of -power status flag **332** if

11 the selected previous  $R$  value exceeds the current  $R$  value by more than the

12 value of an internally stored, preselected fixed parameter RDELTA for one or

13 more consecutive measurement cycles. The signaling device activation logic **36**

14 is configured to not activate the signaling devices **37** if the status flag **332** is set

15 to indicate a transmitter loss-of-power condition. The loss-of-power status bit

16 also activates a master reset of the entire receiver module digital IC **32**. For pet

17 containment applications, the previous  $R$  value used by the loss-of-power

18 detection logic **308** is the R3 sample **383**, and the value of RDELTA is typically

19 in the range of 1 to 1.5 times the value of the RTHLD parameter.

20 According a wireless pet containment system has been shown and

21 described. Those skilled in the art will recognize that the embodiments of the

22 wireless pet containment system described herein can be varied without

23 departing from the spirit and scope of the present invention. For example,

24 where component values are referenced, those values are intended to be

25 representative of one embodiment of the wireless pet containment system

26 according to the present invention and not a limitation on acceptable component

27 values. Further, while a number of components are described as being

28 combined in a single integrated circuit, those skilled in the art will recognize that

29 the functions included on the integrated circuit can be realized in other

30 implementations, for example, using discrete components. While sacrificing

31 small size, other implementations are acceptable alternatives where size and

32 power consumption are not primary considerations.

1        While several embodiments have been shown and described, it will be  
2    understood that it is not intended to limit the disclosure, but rather it is  
3    intended to cover all modifications and alternate methods falling within the  
4    spirit and the scope of the invention as defined in the appended claims.